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UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION

PATENT NO. : 7,082,075 B2  
DATED : July 25, 2006 10/804249  
INVENTOR(S) : Beth E. Skidmore

It is certified that error appears in the above identified patent and that said Letters Patent is hereby corrected as shown below:

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
<i>Title</i> <del>First</del> page, Column 2	Cited references 6,597,621, 6,603,705, 6,754,117, 6,754,118, 6,760,274 and 6,845,432 all read B1	Cited references 6,597,621, 6,603,705, 6,754,117, 6,754,118, 6,760,274 and 6,845,432 should read B2
<i>Title</i> <del>Second</del> page 2, Column 1	Cited references 6,862,229, 6,906,960, 6,928,023 and 6,965,980 all read B1	Cited references 6,862,229, 6,906,960, 6,928,023 and 6,965,980 should read B2

~~Drawing Sheet 1,  
Figure 1: Reference  
number 10 should be  
added to reflect the  
entire memory  
device.~~

Delete drawing sheet 1 and sub-  
stitute the attached drawing sheet  
1. Therefor

~~Drawing Sheet 2,  
Figure 2: Reference  
number 128d should  
reference the sense  
amplifier box  
entitled, "SA-3".~~

Delete drawing sheet 2, and substitute  
the attached drawing sheet 2 therefor

Delete the title page showing an illustrative  
figure, and substitute the attached Title page  
therefor.

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Column 1, Line 31

"sense amplifiers provided"

--sense amplifier provided--



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(12) **United States Patent**  
**Skidmore**

(10) **Patent No.:** **US 7,082,075 B2**  
(45) **Date of Patent:** **Jul. 25, 2006**

(54) **MEMORY DEVICE AND METHOD HAVING  
BANKS OF DIFFERENT SIZES**

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(73) **Assignee:** **Micron Technology, Inc., Boise, ID  
(US)**

(\*) **Notice:** Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** **10/804,249**

(22) **Filed:** **Mar. 18, 2004**

(65) **Prior Publication Data**  
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(51) **Int. Cl.**  
**G11C 8/00** (2006.01)

(52) **U.S. Cl.** ..... **365/230.03; 365/189.08;**  
365/230.08

(58) **Field of Classification Search** ..... **365/230.01,**  
365/230.03, 230.05, 230.08, 189.08  
See application file for complete search history.

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(Continued)

*Primary Examiner*—Tuan T. Nguyen

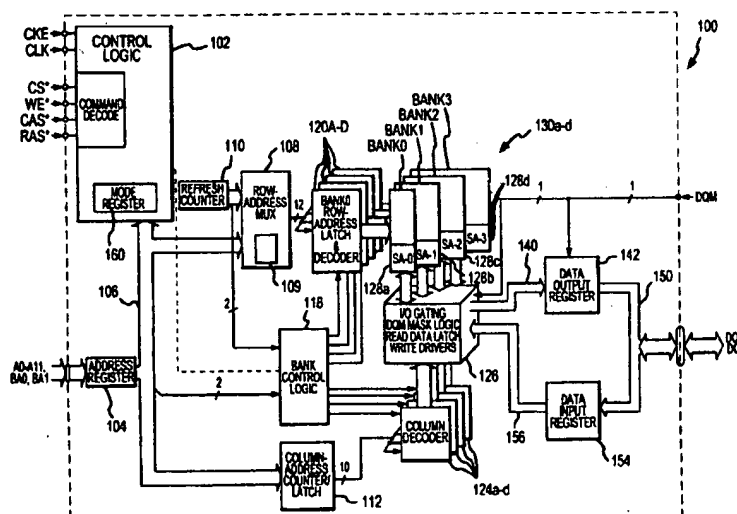
*Assistant Examiner*—Hien Nguyen

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(57) **ABSTRACT**

A memory device, such as a synchronous random access memory device, includes four banks of memory cells arranged in rows and columns. Different numbers of columns of memory cells are contained in each of the four banks. The bank in which an item of data are stored is determined by either the memory device, a memory controller or a processor based on one or more of several factors. For example, the bank in which the data are stored may be determined by the nature of the data or the length of data bursts written to or read from the memory device. Alternatively, the bank in which the data are stored may be determined based on the source of data written to the memory device or destination for data read from the memory device.

**27 Claims, 3 Drawing Sheets**



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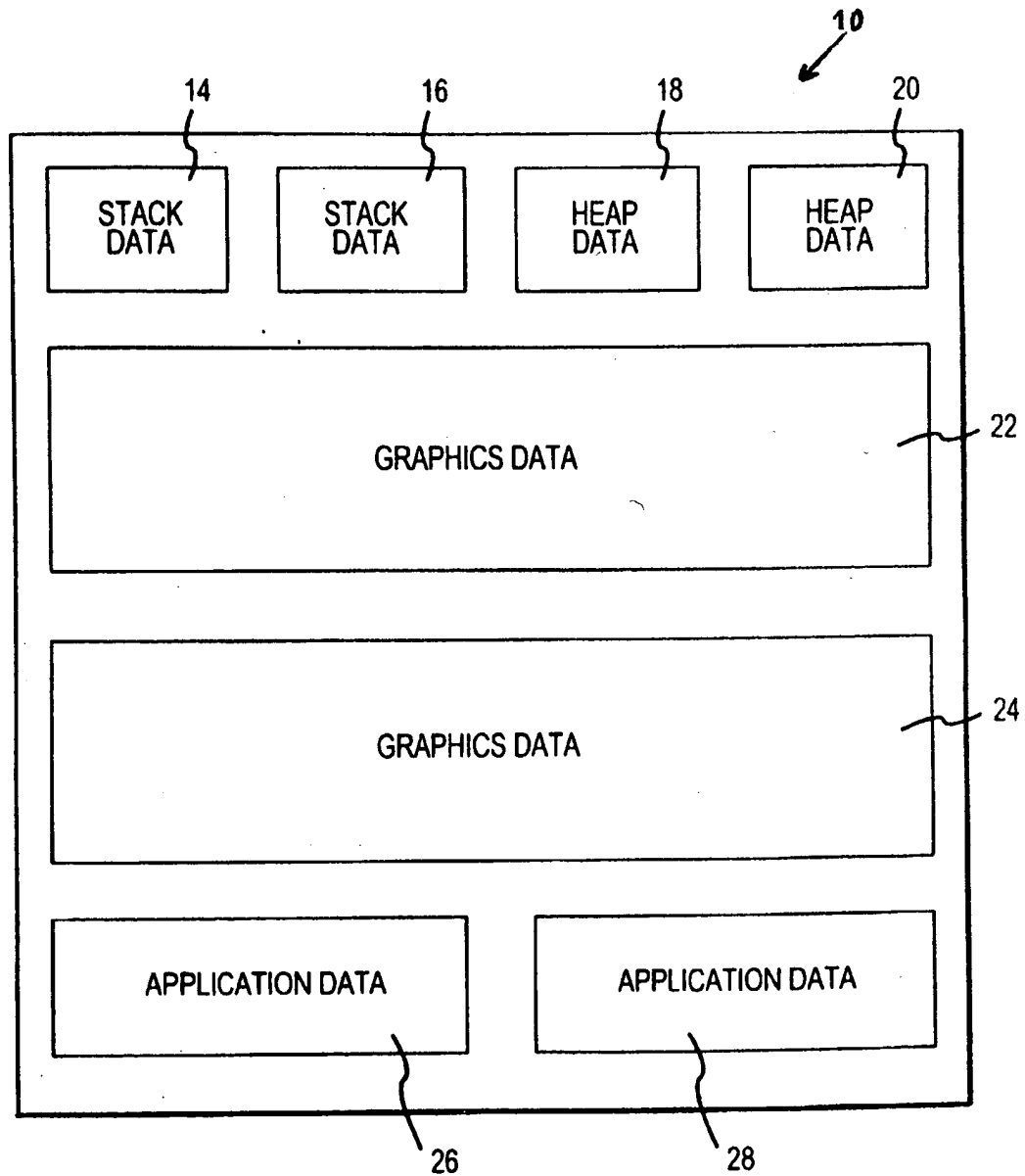


FIG. 1

**FIG. 2**

Column 2, Lines 46-47	"columns of memory cells of memory cells."	--columns of memory cells.--
Column 2, Line 59	"banks 14, 16 18 and 20"	--banks 14, 16, 18 and 20--
Column 3, Lines 15-16	"in FIG. 1 is a"	--in FIG. 2 is a--
Column 3, Line 42	"array 130a-d"	--memory bank 130a-d--
Column 3, Line 46	"arrays 130a-d"	--memory banks 130a-d--
Column 4, Line 57	"in the arrays 120a-d"	--in the banks 130a-d--
Column 5, Line 64	"memory controller 230"	--system controller 214--
Column 6, Lines 5-6	"memory controller 230"	--system controller 214--
Column 7, Lines 32-33	"banks at a location determined"	--banks at a location determined--
Column 8, Line 65	"command signals;"	--command signals; and--

MAILING ADDRESS OF SENDER:

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